

CLAIMS

- 5 1. A semiconductor device comprising:
a substrate having pads;
a first semiconductor chip mounted on said
substrate and having pads;
a plate member arranged on said first
semiconductor chip and having an end at an inward
position of said first semiconductor chip from the pads;
a second semiconductor chip arranged on
10 said plate member and having pads;
a structure electrically connecting said
pads of said first semiconductor chip and said pads of
said second semiconductor chip to said pads of said
substrate; and
15 a seal member sealing said first
semiconductor chip and said second semiconductor chip.
- 20 2. A semiconductor device according to claim 1,
wherein said structure electrically connecting said pads
of said first semiconductor chip and said pads of said
second semiconductor chip to said pads of said substrate
comprises wires.
- 25 ~~3. A semiconductor device according to claim 1,
wherein said plate member has a side surface exposed to
the outside said seal member through a side surface
thereof.~~
4. A semiconductor device according to claim 1,
wherein said plate member comprises a plurality of
laminated layers.
- 35 ~~5. A semiconductor device according to claim 1,
wherein said plate member includes pads and said
structure electrically connecting said pads of said first
semiconductor chip and said pads of said second
semiconductor chip to said pads of said substrate
includes members electrically connecting at least one of
said pads of said second semiconductor chip and said pads
of said second semiconductor chip to said pads of said
plate member and members electrically connecting said~~

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6. A semiconductor device according to claim 1, wherein said plate member has a first portion covered by said first and second semiconductor chips, and a second portion protruding from said first and second semiconductor chips, said second portion having a side surface flush with a side surface of the seal member.

6. A semiconductor device according to claim 1,
wherein said plate member has a first portion covered by
said first and second semiconductor chips, and a second
5 portion protruding from said first and second
semiconductor chips, said second portion having a side
surface flush with a side surface of the seal member.

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